A Configurable Radiation Tolerant Dual-Ported Static RAM macro, designed in a 0.25 µm CMOS technology for applications in the LHC environment.

K. Kloukinas, G. Magazzu, A. Marchioro

CERN EP division, 1211 Geneva 23, Switzerland
Kostas.Kloukinas@cern.ch

Abstract

A configurable dual-port SRAM macro-cell has been developed based on a commercial, 0.25 µm, 3 metal layer, CMOS technology. Well-established radiation tolerant layout techniques have been employed in order to achieve the total dose hardness levels required for the LHC experiments. The presented SRAM macro-cell can be used as a building block for on chip readout pipelines, data buffers and FIFOs. The design features synchronous operation with separate address and data busses for the read and write ports, thus allowing the execution of simultaneous read and write operations. The macro-cell is configurable in terms of word counts and bit execution of simultaneous read and write operations. The and data busses for the read and write ports, thus allowing the design features synchronous operation with separate address and data busses for the read and write ports, thus allowing the execution of simultaneous read and write operations. The macro-cell is configurable in terms of word counts and bit execution of simultaneous read and write operations. The test results are being reported.

Several front-end ASICs for the LHC detectors are now implemented in a commercial 0.25 µm CMOS technology using well established special layout techniques [1] [2] to guarantee robustness against total dose irradiation effects over the lifetime of the LHC experiment. In many cases these ASICs require the use of rather large memories in readout pipelines, readout buffers and FIFOs. The lack of SRAM blocks and the absence of design automation tools for generating customised SRAM blocks that employ the radiation tolerant layout rules are the primary motivating issues for the work presented in this article.

This paper presents a size-configurable architecture suitable for embedded SRAMs in radiation tolerant, quarter-micron, ASIC designs. Physical layout data consist of a memory-cell array and abutted peripheral blocks: column address decoder, row address decoder, timing control logic, data I/O circuitry and power line elements to form power line rings. Each block is size configurable to meet the demand on word counts and data bits, respectively.

To minimize the macro-cell area a single port memory cell is used based on a conventional cross-coupled inverter scheme. Dual-port functionality is realized with internal data and address latches, placed closely to the memory I/O ports, and a time-sharing access mechanism. The design allows both read and write operations to be performed within one clock cycle. The scalability of the presented SRAM macro-cell is accomplished with the use of replica memory cells and self-timed control circuits.

The presented memory macro-cell has already been embedded in a number of detector front-end ASIC designs for the LHC experiment, with configurations ranging from 128words x 153bits to 64Kwords x 9bits.

II. CIRCUIT DESIGN

A. Memory Architecture

The internal architecture of the SRAM design is shown in Figure 1. It consists of an array of Static Memory Cells coupled with the necessary Write Drivers and Read Logic circuitry, a Row Decoder, a Column Decoder, a set of registers for the address and the data input ports, a latch for the data output port and a Timing Logic circuitry controlling the operation of the SRAM macro-cell.

The cells in the memory array are accessed by the Row Decoder that selects the wordline and the Column Decoder that selects the appropriate bitlines. The Row Decoder has a fixed size of 128 wordlines and its decoding function is hardwire-configured with via-hole programming on a 7-bit complementary bus. The 7 most significant bits of the desired memory cell address are routed to the Row Decoder and the rest (n-7) address bits are routed to the Column Decoder.

![Figure 1 : Block diagram of the Dual Port SRAM.](image-url)
The SRAM cell was implemented as a true dual-port cell using memory cell design was first introduced in [3]. In that design, the layout of the memory cell is shown in Figure 3. The memory cell is based on a conventional cross-coupled inverters design. The cell uses PMOS pass transistors as access devices, since they are smaller than enclosed NMOS transistors. In addition special care was applied in the design of NMOS transistors, to make them even smaller than what a conventional enclosed NMOS transistor requires. The resulting size of the memory cell is only 5.60µm x 8.42µm. The layout of the memory cell is shown in Figure 3. The memory cell design was first introduced in [3]. In that design, the SRAM cell was implemented as a true dual-port cell using 8 transistors. By eliminating the 2 access transistors of the second port we gain in area a factor of 18% without compromising functionality or performance.

The scalability of the presented SRAM macro-cell is accomplished with the use of replica rows of memory cells and bit-lines that create reference signals whose delays tracks that of the word-lines and bit-lines [5]. An extra row containing replica memory cells (Dummy Wordline) is placed in the memory array to track the wordline charge-discharge delay that varies with the size of the macro-cell. It may also vary with temperature and process variations. An extra column containing replica memory cells (Dummy Bitlines) is placed to mimic the bitlines delay. These “reference signals” track the delay of the actual wordline and bitlines accurately, making the memory robust while preserving performance. The timing control of the memory operations is handled by an asynchronous self-timed logic (Timing Logic) that adjusts the timing of the operations to the delays of the reference signals.

C. Dual Port Functionality

The dual-port functionality is realized by employing a time sharing access of the memory array. The read and write operations are handled in one clock cycle. In Figure 2, clock cycle #1 represents a write operation, cycle #2 a read and cycle #4 a read/write operation.

Figure 2 : Timing diagram of the Dual Port SRAM Interface.

D. Replica Techniques

Figure 3 : Layout of the SRAM memory cell using radiation tolerant layout techniques.

The scalability of the presented SRAM macro-cell is accomplished with the use of replica rows of memory cells and bit-lines that create reference signals whose delays tracks that of the word-lines and bit-lines [5]. An extra row containing replica memory cells (Dummy Wordline) is placed in the memory array to track the wordline charge-discharge delay that varies with the size of the macro-cell. It may also vary with temperature and process variations. An extra column containing replica memory cells (Dummy Bitlines) is placed to mimic the bitlines delay. These “reference signals” track the delay of the actual wordline and bitlines accurately, making the memory robust while preserving performance. The timing control of the memory operations is handled by an asynchronous self-timed logic (Timing Logic) that adjusts the timing of the operations to the delays of the reference signals.

Figure 4 : Design of the Replica Word-Line and Bit-Lines.
inverted bitlines, but are read using a single bitline through an asymmetric inverter. By substituting the sense amplifier with a simple inverter we gain in power consumption and have a stable operation even at low power supply voltage.

E. Divided Word Line Architecture

To minimize further the power consumption, we have adopted a wordline selection scheme called Divided Wordline Decoding (DWL) [6]. The wordline has a hierarchical structure of two levels, namely the Global and the Local wordlines as shown in Figure 5. Part of the address is decoded to activate the Global Wordline and the remaining address bits are decoded by the Block Pre-Decoder and activate the vertical block select lines. The Local Wordline Buffers receive the select signals from the Block Pre-decoder logic and drive the selected Local Wordline in a selected block for read and write operations. The non-accessed portions of the memory remain in the precharge state, thus reducing the power consumption. Wordline selection time is also improved since the RC delay in each divided wordline is small due to the short length.

Figure 5 : The Divided Word Line (DWL) architecture in the SRAM.

F. Operation and Timing

Although the SRAM macro-cell is externally synchronous for the user application, the internal timing of the various control signals is completely asynchronous and self-timed. The Timing Logic uses a combination of hand-shaking and transition detection to realize internal timing loops that are initiated by the edges of the system clock and terminate upon completion of the operation. Figure 6 shows the timing loops for a read followed by a write operation. The read operation is performed during the high period of the clock (clk) and the write during the low. The operation is completely static. All control signals are forced back to their initial state so that the wordline and bitlines are immediately precharged to prepare for the subsequent tasks.

A read is performed by starting with both BL and BL low and the Row Decoder in the precharge state. Asserting the WL_pc signal sets the Row Decoder to the evaluate state and the desired Global Wordline is selected. With the combination of the appropriate Block Select signal the desired Local Wordline is selected. At this time the data in the cell will pull either the BL or the BL line high. The condition is detected by the NOR gate and the BL0 signal goes low signifying that the data can be safely latched and that the Row Decoder can return to the precharged state. At this time the reference signals WLdummy and LWLdummy are subsequently de-asserted signalling that the bitlines can safely return to the precharge state.

Figure 6 : Timing diagram for a Read and a Write operation.

To write into the cell, data are placed on the BL and BL by the Write Logic. Then the wordline is activated. This will force the memory cell to flip into the state represented on the bitlines. The cycle ends with the wordlines and bitlines returning to the precharged state.

A large part of the operating power consumption of a static memory is due to the charging and discharging of the column and bit-line loads. To reduce the wasted power during standby periods the Timing Logic does not initiate bitline and wordline precharge cycles if there is no access to the memory.

III. MACRO-CELL IMPLEMENTATIONS

A. Cell Library

The design approach was taken so as to allow the use of as many common circuits and circuit blocks as possible in all supported configurations. The physical layout library consists of a Memory-Cell Array, Write Drivers and Read Logic blocks, a 129 line Row Decoder, a 129 line Wordline Buffer, a Data In register, a Data Out latch, an Address Register/Multiplexer and a Timing Logic. All the blocks in the library apart from the Timing Logic, the Row Decoder and Wordline Buffer are size configurable to meet the demand on word counts and data bits. Each block can be configured by abutting a certain number of times a leaf library cell.

The SRAM macro-cell uses 3 metal layers. The 1st metal layer is used for local interconnections in the leaf cells. The bit-lines and power lines run vertically on the 2nd level metal, and the global and local word-lines are run horizontally on the 3rd level metal layer.
B. Macro-Cell Assembly

Figure 7 shows the floorplan of the common building blocks and typical configurations [(a) 128words X 36bit, (b) 512words X 18bits and (c) 4Kwords X 9bits] of the SRAM macro-cell. The Memory-Cell Array consists of Memory-Cell Blocks. Each Memory-Cell Block is divided into Memory-Cell Columns each of which comprises 128 words. A Memory-Cell Block can have from one up to four Memory-Cell Columns that share a common Wordline Buffer Block. The smallest memory size that can be composed is 128 words X 9 bits, making use of a single Memory-Cell Column. For bigger memories, the Memory-Cell Array can be split in two halves and placed on both sides of the Row Decoder Block. All the peripheral circuits (Timing Logic, Address and Data Input Registers, Data Output Latch) are placed on the right side of the Memory-Cell Array.

IV. FABRICATION AND EXPERIMENTAL RESULTS

A. SRAM Chip Fabrication

To prove the concept of the SRAM macro-cell scalability and to evaluate the performance of the proposed circuitry two test chips were designed and fabricated using a commercial 0.25μm, 3 metal layer, CMOS technology.

Figure 8 shows a microphotograph of the fabricated 1K X 9bit SRAM macro-cell. The size of the macro-cell is 560μm X 1,300μm and contains two Memory-Cell Blocks and peripheral circuitry. Each block is configured as 512 X 9bit and is composed of four 128 X 9bit Memory-Cell Columns. Figure 9 shows a microphotograph of the fabricated 4K X 9bit SRAM macro-cell. The size of the macro-cell is 1,850μm X 1,300μm and contains eight 512 X 9bit Memory-Cell Blocks, each composed of four 128 X 9bit Memory-Cell Columns.

B. Experimental Results

Both test chips were tested and found functional up to the frequency of 70MHz for simultaneous Read/Write operations. The typical read access time (t_{ac}) of the 1Kword X 9bits was found 4.5 nsec and that of the 4Kword X 9bits 7.5 nsec. A Schmoo plot of the 4Kwords X 9bits SRAM access time versus the power supply voltage for a checkerboard test pattern is shown in Figure 10. A stable operation over a wide range of power supply voltage was achieved. The chip was operating at 50MHz without faults from 2.0 to 2.7 V, demonstrating design robustness.

The power dissipation measurements for different operating modes of the 4Kwords X 9bits test chip are shown in Figure 11. For the Read, Write and Read/Write operations a checkerboard test pattern has been used. In Idle mode there were no accesses to the memory while the system clock was running with the address and data input ports changing in every clock cycle. In Standby mode the system clock was running but the input ports were kept at a fixed state. Table 1 summarizes the measurement results. The power dissipation in the Idle mode is higher than in the Standby mode because of the activity in the registers of the address and data input ports. Idle operation is smaller than Read, Write and Read/Write operations in power dissipation, demonstrating the power reduction benefit of the static design of the Timing Logic.
Figure 10: Schmoo plot of the access time versus the power supply voltage for the 4Kwords X 9bits SRAM macro-cell using a checkerboard test pattern at 50MHz.

Figure 11: Power Dissipation measurements for the 4Kwords X 9bits SRAM test chip at 2.5Volts.

Table 1: Power dissipation figures for the 4Kwords X 9bits SRAM test chip.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Power (µW/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby</td>
<td>0.10</td>
</tr>
<tr>
<td>Idle</td>
<td>1.90</td>
</tr>
<tr>
<td>Read</td>
<td>7.40</td>
</tr>
<tr>
<td>Write</td>
<td>10.60</td>
</tr>
<tr>
<td>Read/Write</td>
<td>14.05</td>
</tr>
</tbody>
</table>

Both test chips were tested for total ionising dose effects using an X-ray source. The chips were irradiated in three steps to 1 Mrad, 5 Mrad and 10 Mrad (SiO₂), at a constant dose rate of 21.2 Krad/min. The chips were annealed for 24 hours at room temperature. They were kept under bias in standby mode during the irradiation and the annealing period. A set of measurements were carried out after each step. The results showed that there was no measurable performance degradation in terms of maximum operating frequency and read access time and there was no increase in the circuit power dissipation.

V. Conclusions

A radiation tolerant SRAM macro-cell has been developed and implemented in a commercially available 0.25 µm, 3 metal layer, CMOS technology. The scalability of the macro-cell has been demonstrated by means of two test chips, carrying two macro-cell configurations of different memory sizes, which were fabricated and tested successfully. The experimental results show that our proposed design can be used in embedded applications for detector front-end ASICs in the LHC experiment environment.

This work has been primarily initiated for the needs of the “Kchip” ASIC for the CMS ECAL Preshower detector. The modularity and scalability of the macro-cell allowed the generation of SRAM configurations suited for a number of other ASICs used in the LHC experiment detectors. A list of ASICs that are currently making use of the presented macro-cell is shown in Table 2.

Table 2: Application of the SRAM macro-cell in various ASICs for the front-end electronics in the LHC experiments.

<table>
<thead>
<tr>
<th>Chip Name</th>
<th>LHC Detector</th>
<th>Laboratory</th>
<th>Config.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCAC</td>
<td>ATLAS tracker</td>
<td>Columbia Univ.</td>
<td>128 X 18</td>
</tr>
<tr>
<td>DTMR0C</td>
<td>ATLAS TRT</td>
<td>CERN</td>
<td>128 X 153</td>
</tr>
<tr>
<td>MCC</td>
<td>ATLAS pixel</td>
<td>INFN Genova</td>
<td>128 X 27</td>
</tr>
<tr>
<td>AMBRA</td>
<td>ALICE Silicon Drift</td>
<td>INFN Torino</td>
<td>16K X 9</td>
</tr>
<tr>
<td>CARLOS</td>
<td>ALICE Inner Tracker</td>
<td>INFN Bologna</td>
<td>256 X 9</td>
</tr>
<tr>
<td>Kchip</td>
<td>CMS Preshower</td>
<td>CERN</td>
<td>1K X 18, 128 X 18</td>
</tr>
<tr>
<td>SYNC</td>
<td>LHCb Muon system</td>
<td>INFN Cagliary</td>
<td>236 X 9</td>
</tr>
</tbody>
</table>

VI. References


